DSPCOMMPCIUM
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Suite56™ PCI Command Converter User's Manual

The Freescale Suite56™ PCI command converter is an interface device that, with the assistance of the Suite56 DSP software development tools debugger, allows you to send and receive information from your host system to a DSP-based system. The interface extends from the PCI bus on the host system through a target interface module to the DSP via a JTAG connection. This manual describes the operating environment and the functionality of the PCI command converter.

CONTENTS

1 General Description 2
2 Operating Environment 2
2.1 Windows PC Requirements 3
2.2 Hewlett Packard Workstation Requirements 3
2.3 Sun Ultra Workstation Requirements 3
3 Functional Description 3
3.1 Command Converter Interface Connector 4
3.2 Multiple Target Connections 5
3.3 TCK Drive and Timing Considerations 6
3.4 Resetting Target DSP Devices 7

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1 General Description

The Suite56 PCI command converter is used for designing, debugging, and evaluating DSP-based systems. **Figure 1** shows how the PCI command converter can be connected in a target system configuration and used as a hardware evaluation tool or as a software accelerator.

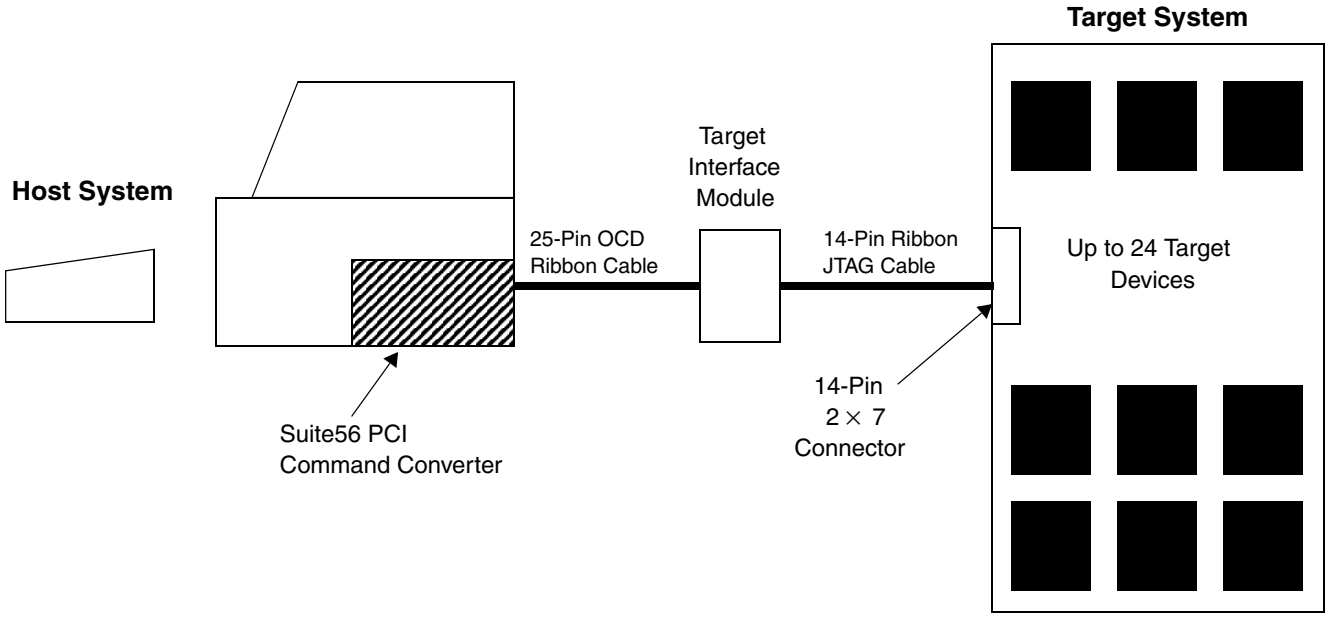


Figure 1. Command Converter to Target System Configuration

The target system in **Figure 1** can be a Freescale DSP application or evaluation board, or any user-defined target system. The user-defined target hardware must have an access point for the 14-pin JTAG ribbon cable, which can be as simple as a 2-row × 7-set of test points. The PCI command converter provides a physical link between the host system and the target via a PCI bus connection on the host card. This link translates the high-level debugger commands into JTAG signals that enable the host system to reset, interrupt, and send commands to the target DSP.

2 Operating Environment

The Freescale DSP Suite56 software development tools for the PCI command converter support the following three host systems:

- Windows PC
- Hewlett Packard workstations
- Sun™ Ultra workstations

2.1 Windows PC Requirements

The minimum hardware requirements for using the Freescale DSP Suite56 software development tools debugger on a Windows PC are as follows:

- Windows PC (Pentium® class processor, or higher)
- Windows® 95 operating system with 16 MB of RAM, Windows® 98 operating system with 32 MB of RAM, or Windows NT 4.0 operating system with 32 MB of RAM

- CD-ROM drive
- Mouse and keyboard
- Hard drive with 50 MB of free space
- Free PCI bus slot

2.2 Hewlett Packard Workstation Requirements

The minimum hardware requirements for using the Freescale DSP Suite56 software development tools debugger on an HP Workstation include the following:

- HP workstation running HP-UX version 9.05 or 10.20 (or higher)
- 32 MB of RAM
- CD-ROM drive
- Hard drive with 50 MB of free space
- Mouse and keyboard
- Free PCI bus slot

2.3 Sun Ultra Workstation Requirements

The minimum hardware requirements for using the Freescale DSP Suite56 Software Development Tools Debugger on a Sun Ultra Workstation include the following:

- Solaris™ Release 2.5.1 (or higher)
- 32 MB of RAM
- CD-ROM drive
- Hard drive with 50 MB of free space
- Mouse and keyboard
- Free PCI bus slot

3 Functional Description

The Suite56 PCI command converter interacts with the target DSP with the assistance of the Suite56 software development tools debugger and the user's host system. The host system interface consists of a C program that sends commands via a PCI bus to the Suite56 PCI command converter. Commands entered from the host system keyboard are parsed, and a series of low-level command packets are sent to the PCI command converter. The PCI command converter translates these low-level command packets into one or more JTAG signals and OnCE commands that are transferred to the target DSP via its JTAG port. The JTAG port provides the necessary control to the target so programs can be loaded or saved, registers read or modified, and hardware breakpoints set or cleared.

3.1 Command Converter Interface Connector

The target application board must have a 14-pin connector to interface to the command converter controller. This interface comprises eight signals and three ground connections on a 7-row × 2-column male pin header, which are spaced on one-tenth inch centers as illustrated in **Figure 2**.

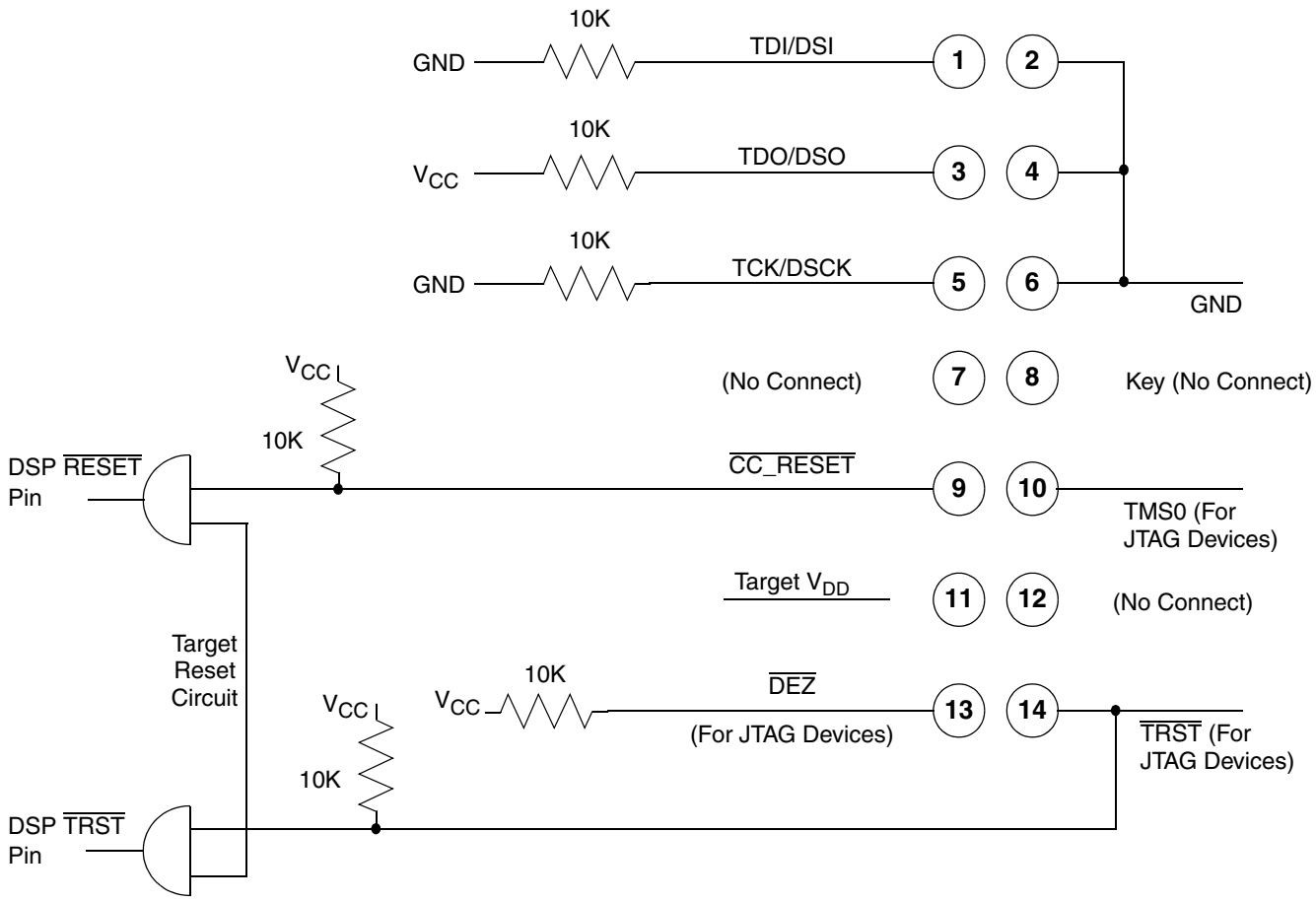


Figure 2. Target V_{DD} System JTAG/OnCE™ Interface Connector

Figure 2 may not represent the exact JTAG/OnCE configuration needed for every DSP due to possible differences in internal resistors on the pins. For information on internal resistors, see the data sheet for your DSP device.

Since the target system has a resident reset circuit, an AND gate-in-series is recommended with the $\overline{\text{CC_RESET}}$ signal to allow the target DSP to be reset with a valid V_{OL} level from either the target-reset circuit or the command converter. The pull-down resistors prevent false signals from being propagated to the JTAG/OnCE circuit when the test data input/debug serial input (TDI/DSI) and test data clock/debug serial clock (TCK/DSCK) lines are active. The test data out/debug serial output (TDO/DSO) pull-up is designed to deassert the Debug Acknowledge signal from the OnCE circuit.

Figure 3 shows the connector coming from the target interface module via a 14-pin ribbon cable. When viewed with pin 8 (keyed) on the right side, this plug connector has all odd numbers on the left side and all even numbers on the right side when viewed from the top. Spacing between pins is one-tenth inch.

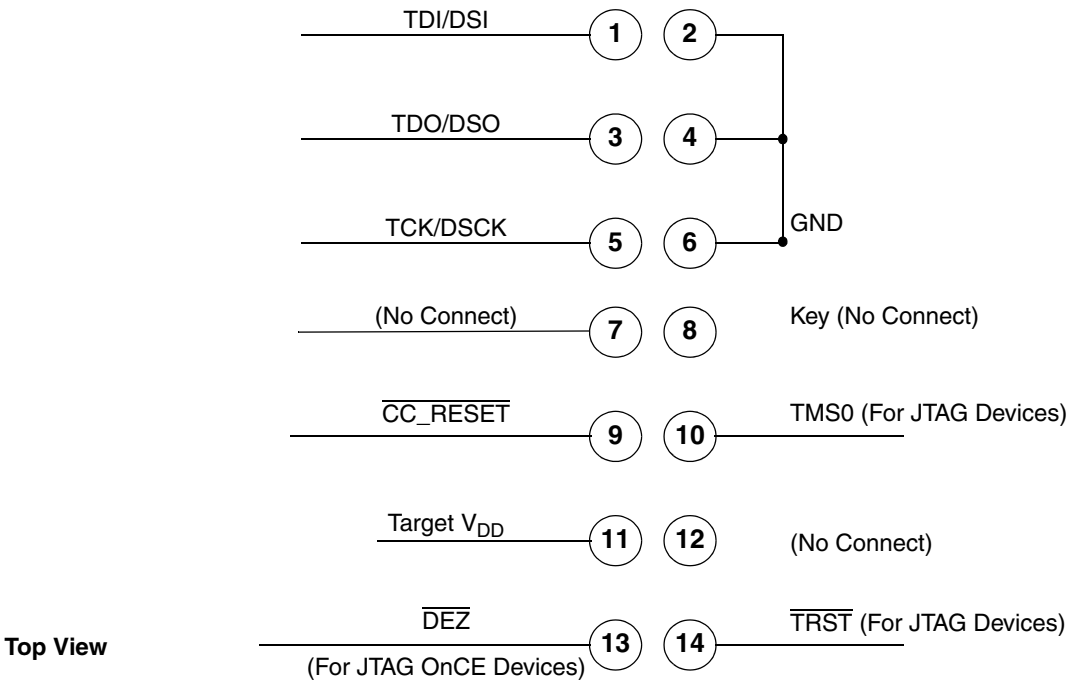


Figure 3. Target Interface Module 4-Pin JTAG/OnCE Connector

3.2 Multiple Target Connections

Multiple target devices can be connected in a series, allowing a single command converter, JTAG/OnCE connector to control multiple devices, as shown in **Figure 4**. Data flows from the JTAG host into each JTAG implementation through TDI, out through TDO, and into TDI in the next device, eventually returning to the JTAG host.

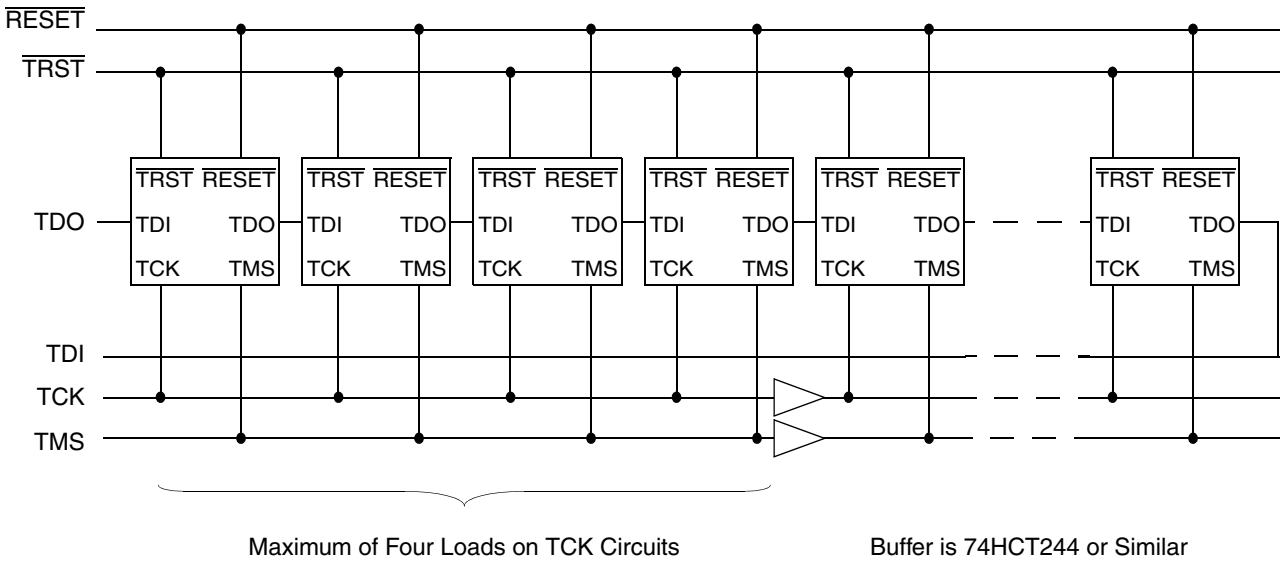
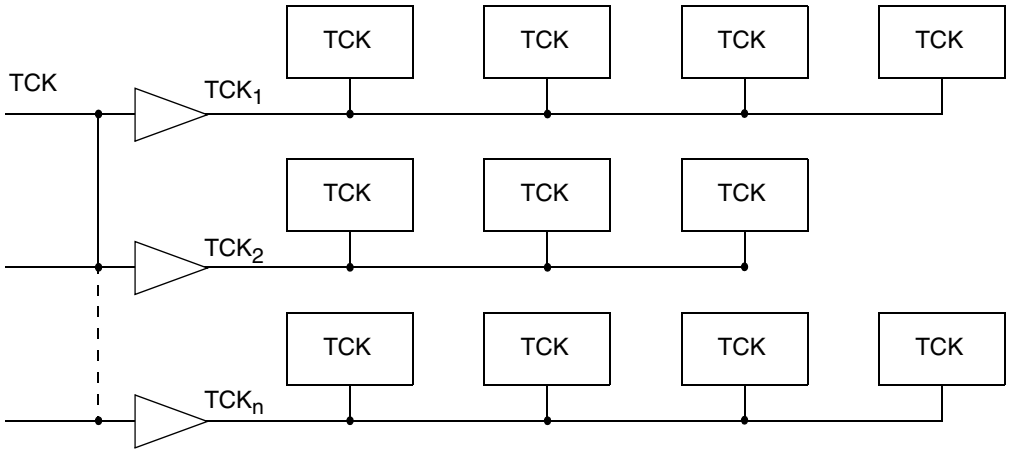


Figure 4. Multiple JTAG Target Connections (Serial Method)

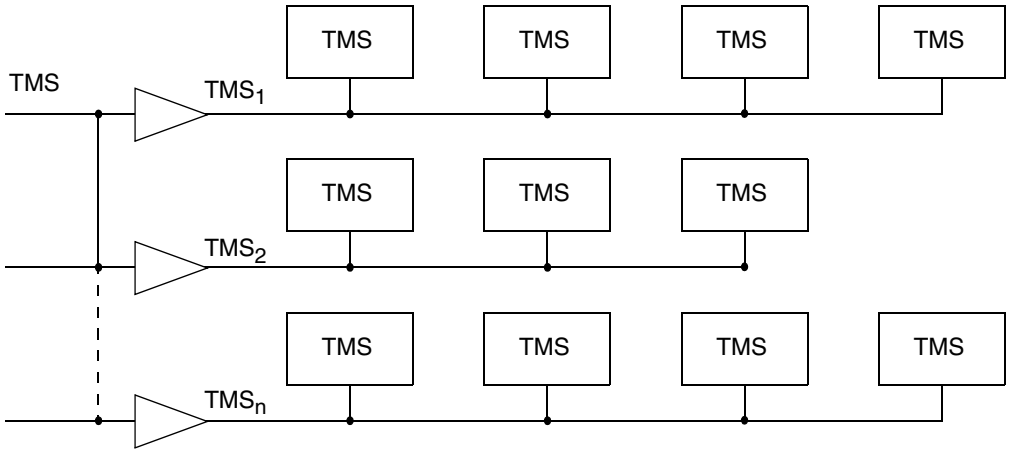
3.3 TCK Drive and Timing Considerations

The signals from the command converter are TDO, TCK, TMS, and $\overline{\text{TRST}}$. The TCK signal requires fast rise and fall times dictated by the TCK pin timing specification, so attention must be given to the drive capability of the circuits driving this signal. When the TCK and TMS circuits are driven with a large number of target devices, you must pay attention to the rise and fall times of TCK and TMS. Excessive capacitance may cause communication problems when driving a single circuit that connects multiple TCK or multiple TMS input pins. Excessive capacitance can also cause communication problems with a single circuit connecting multiple TMS input pins.

Acceptable transition times may be achieved for TCK and TMS by driving no more than four JTAG inputs from each buffered output. This may be achieved with two configurations. **Figure 4** shows one method. Here (in effect) one signal connects each of the TCK inputs, and one signal connects each of the TMS inputs. A buffer is placed in the circuit after each fourth input at most, to restore the signal quality for subsequent inputs. The propagation delay of the buffer is not significant. **Figure 5** shows two possible configurations of a second method that also enables signal quality to meet the requirements. In configuration Number 1, the signal is split and buffered into a number of parallel TCKx signals. Each of these signals can drive up to four TCK inputs.



Configuration 1: Fan Out of TCK at Source



Configuration 2: Fan Out of TMS at Source

Figure 5. Multiple JTAG Connectors (Parallel Method)

In Configuration Number 2, the signal is split and buffered into a number of parallel TMSx signals. Each of these signals can drive up to four TMS inputs.Each method is equally valid. The choice of methods depends on the project.

3.4 Resetting Target DSP Devices

The $\overline{\text{RESET}}$ signal and $\overline{\text{TRST}}$ signals from the command converter typically connect to all target DSP devices on a JTAG chain. All these DSP devices are reset when $\overline{\text{RESET}}$ and $\overline{\text{TRST}}$ are asserted by the debugger command FORCE R. Execution control is established immediately after deassertion of $\overline{\text{TRST}}$ and before any instructions execute. This sequence of events is illustrated in **Figure 6**.

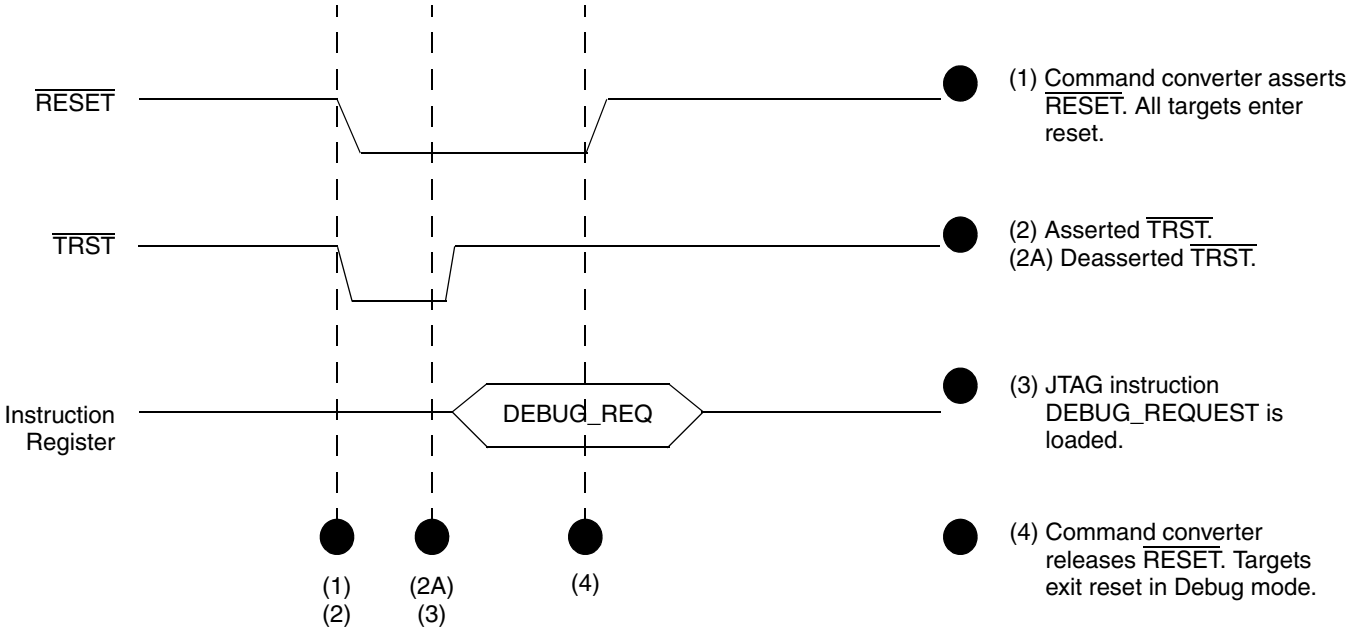


Figure 6. Reset JTAG Device with $\overline{\text{RESET}}$ Signal

The JTAG controller is still active after deassertion of $\overline{\text{TRST}}$ during reset and while $\overline{\text{RESET}}$ is held low. The JTAG special instruction DEBUG_REQ is clocked in before $\overline{\text{RESET}}$ is deasserted. When $\overline{\text{RESET}}$ is deasserted, the device immediately goes into Debug mode, and no instructions execute in the DSP.

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